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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,077	10/27/2000	Masahiro Ishida	KPO089	9031

25271 7590 03/14/2005

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 09/699,077	**Applicant(s)** ISHIDA ET AL.	
	Examiner Ayal I Sharon	**Art Unit** 2123	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 03 February 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The reply was filed after the date of filing a Notice of Appeal, but prior to the date of filing an appeal brief. The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

ADVISORY ACTION

1. The Request for Reconsideration has been considered but does NOT place the application in condition for allowance.
2. Applicants requested in the After-Final Request for Reconsideration (filed 2/3/05, p.4, last paragraph) that the Examiner "explain where the TSPC [transient power supply current] testing method is disclosed".
    a. Examiner refers the applicants to the abstract of the Cole reference, which teaches the following:

    "The apparatus provides an operating voltage, V_{DD}, to an IC under test and measures a transient voltage component, V_{DDT}, signal that is produced in response to switching transients that occur as test vectors are provided as inputs to the IC."

    b. Moreover, as cited in the rejection of Claim 1 in the previous Office Action, the Cole reference (col.3, lines 35-46) teaches the following:

    "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC)."

    c. Examiner found, in the previous Office Action, that the "transient voltage component V_{DDT}" testing method corresponds to the Applicant's claimed "transient power supply current" testing method.

    d. Examiner notes that current and voltage are inherently interchangeable via Ohm's law (V=IR).

3. Applicants also requested in the After-Final Request for Reconsideration (filed 2/3/05, p.4, last paragraph) that the Examiner "explain ... what feature is the claimed list of detectable faults, and what feature is believed to generates this list."

   a. As stated in the rejection of Claim 2 in the previous Office Action, the Cole reference (col.3, lines 35-46) teaches the following:

      "... toggling the IC between logic states by providing a vector set of voltage inputs to input pins of the IC ... and identifying ICs having defects or failure mechanisms therein by determining whether the transient voltage component, V_{DDT} exceeds a known value. The known value can be derived from measurements of one or more defect-free ICs using the present invention, or derived from numerical modeling of electrical characteristics of the IC (i.e. from modeling of a design for the IC)."

   b. Examiner interprets that Cole's "... identifiying ICs having defects or failed mechanisms therein ..." corresponds to the Applicants' claimed limitation of " ... generating a list of faults, which are detectable by a transient power supply current testing ..."

   c. The feature in Cole that generates Cole's list of "...ICs having defects or failed mechanism" is "determining whether the transient voltage component, Vddt exceeds a known value."

4. In regards to Claims 11 and 12, the rejection in the previous Office Action stated that:

   The Carmichael reference teaches the insertion of assumed faults into the semiconductor IC (see Section II.A. "Simulation Process"), as well as applying the test pattern is applied to the semiconductor IC with the assumed fault inserted therein (see Section III.A. "Switching Regulator Example"), deciding whether the assumed fault is detectable (see Section III.A. "Switching Regulator Example"), and generating a fault list in which

the detectable faults are registered (see Section III.A. "Switching Regulator Example").

Examiner finds that the "diagnostic test strategy" taught in Section III.A corresponds to the Applicants' "technique that determines whether a particular fault can be detected by TSPC testing" (Req. for Reconsideration, filed 2/3/05, p.5, paragraph 5).